Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations October-2020

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Sketch the internal organization of CPU out with its functionalities and block diagram?	**6M**
	b	With suitable paradigms, describe the Instruction types used in Assembly level languages?	**6M**

OR

2	**a**	Explain the phases involved in Instruction cycle with the help of necessary timing diagrams?	**6M**
	b	Design a relatively simple computer which incorporates 8K RAM, 8K ROM, IO interfacing modules along with processor?	**6M**

UNIT-II

3	**a**	Illustrate the basic requirements for Input and Output communication using a terminal unit such as keyboard and printer.	**6M**
	b	Explain the process for signed magnitude addition and subtraction with flow chart?	**6M**

OR

4	**a**	Using the register transfer notations, explain the Memory-Reference instructions with examples?	**6M**
	b	Implement hardware for multiplying Two fixed- point binary numbers in signed-magnitude representation along with its flowchart?	**6M**

UNIT-III

5	**a**	Implement 4-bit Binary Adder-Subtractor and Binary Increment.	**6M**
	b	Write about hardware organization of micro programmed control unit.	**6M**

OR

6	**a**	Design a 4-bit ALU which performs arithmetic, Logical and shift operations.	**6M**
	b	Explain about address sequencing in control memory with neat diagrams.	**6M**

UNIT-IV

7	**a**	Brief out the hardware organization of Associative memory with diagrams.	**6M**
	b	With a neat schematic, Explain about DMA controller and its mode of data transfer.	**6M**

OR

8	**a**	Discuss the Memory Hierarchy in computer system with regard to Speed, Size & Cost.	**4M**
	b	Classify and describe the possible modes of data transfer to and from peripherals with examples.	**8M**

UNIT-V

9	**a**	Illustrate the behavior of a pipeline using space-time diagram.	**8M**
	b	Differentiate tightly coupled and loosely coupled multiprocessors.	**4M**

OR

10	**a**	Implement a simple pipeline unit for floating addition and subtraction.	**6M**
	b	Explain in detail about crossbar switching and Multistage switching network system.	**6M**

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